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**C Code:**

uint32\_t read\_nvic\_cpuid\_base(

uint32\_t \*reg\_ptr,

uint32\_t \*implementer,

uint32\_t \*variant,

uint32\_t \*partno )

{

uint32\_t reg\_val;

reg\_val = \*reg\_ptr;

\*implementer = (reg\_val >> 24) & 0xFF;

\*variant = (reg\_val >> 20) & 0xF;

\*partno = (reg\_val >> 4) & 0xFFF;

return reg\_val;

}

**Assembly code:**(let r4 contain address of reg\_val,r0 contain \*reg\_ptr,r1 contain \*implementer,r2 contain \*variant and let any register # between 4 and 16 represent a temporary register)

LDR r4,[r0] //reg\_val=\*reg\_ptr

LSR r5,[r4,#24]

AND r6,r5,#oxFF

STR r6,[r1]

LSR r7,[r4,#20]

AND r8,r7,#oxF

STR r8,[r2]

LSR r9,[r4,#4]

LDR r12=oxFFF //FFF is to big to fit in immediate value field

AND r10,r9,r12

STR r10,[r3]

PUSH{r4,r5,r6,r7,r8,r9,r10,r12}

POP {r4,r5,r6,r7,r8,r9,r10,r12}

BX LR //Return from subroutine